

CLAIMS

- 1 1. A method for transmitting a signal digitized with a scanning frequency, with a word width
2 of n bits, from a data source to a data sink in a data transmission system, with an operating
3 frequency, which has at least one channel with a width of m bits, such that n is greater than m , and
4 the operating frequency is greater than the scanning frequency, comprising decomposing each data
5 word of the signal into at least two partial words with a width that is less than m , and that at least
6 two partial words obtained from one data word are transmitted on the channel together with an
7 identifier that identifies the position of the partial word in the original data word.
- 1 2. The method of claim 1, wherein, after transmission on at least one channel, the original
2 data word is reconstructed from the partial data words by means of the identifier.
- 1 3. The method of claim 1, wherein the identifier comprises one bit.
- 1 4. The method of claim 1, wherein as many as a partial data words of one data word are
2 transmitted on one channel if the operating frequency is at least a times the scanning frequency and
3 less than $(a-1)$ times, wherein a is an integer value.
- 1 5. The method of claim 4, wherein a is equal to two.
- 1 6. The method of claim 1, wherein n is equal to fourteen and m is equal to eight.
- 1 7. The method of claim 6, wherein each data word is obtained by rounding to fourteen bits an
2 analog signal scanned with a resolution of sixteen bits.

16. The data source of claim 15, wherein the logic circuit is designed to shift bits 2 to 8 of a 16-bit data word of the digitized signal by one bit to the right, and to enter an identifier as first or respectively second partial word, into the respective least significant bit of the two bytes of the resulting data word.

5 17. A data sink to reconstruct a digitized signal with a word width of n bits, by means of data transmitted on an m bit-wide channel of a data transmission system, such that n is greater than m, comprising a logic circuit to decompose each received data value into a partial word with a width less than m bits and an identifier, and to recombine the partial words to an original data word of the digitized signal by means of the identifier.

10 18. The data sink of claim 17, wherein the logic circuit is designed to combine two received data values with a width of $m = 8$ bits to a 16-bit-wide data word, and to shift the least significant byte of the data word by one bit to the left.

15 19. The data sink of claim 18, comprising means for setting the two least significant bits of the recombined data word to a specified value.